

First Named Inventor	Andrei Mihnea	INFORMATION DISCLOSURE STATEMENT FORM PTO-1449
Serial No.	10/636,181	
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Group Art Unit	2801	
Examiner Name	Unknown	
Confirmation No.	1762	
Attorney Docket No.	400.237USO	
Title: METHOD FOR ERASING AN IMAGE		Sheet 1 of 7

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Title: METHOD FOR ERASING AN NROM CELL		Sheet 4 of 7

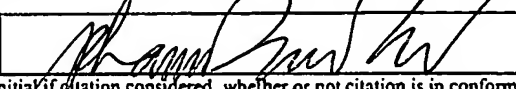
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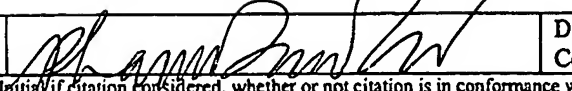
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